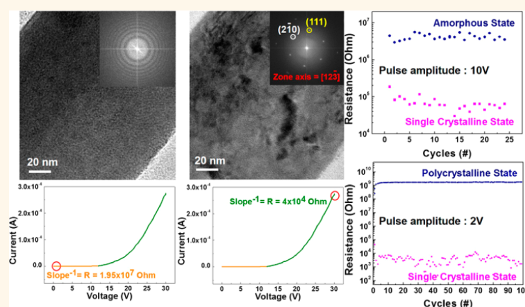
Dynamic Observation of Phase Transformation Behaviors in Indium(III) Selenide Nanowire Based Phase Change Memory

Yu-Ting Huang,[†] Chun-Wei Huang,[†] Jui-Yuan Chen,[†] Yi-Hsin Ting,[†] Kuo-Chang Lu,[‡] Yu-Lun Chueh,[§] and Wen-Wei Wu[†,*]

[†]Department of Materials Science and Engineering, National Chiao Tung University, No. 1001, University Road, Hsinchu 300, Taiwan, [‡]Department of Materials Science and Engineering, National Cheng Kung University, Tainan 701, Taiwan, and [§]Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu 300, Taiwan

ABSTRACT Phase change random access memory (PCRAM) has been extensively investigated for its potential applications in next-generation nonvolatile memory. In this study, indium(III) selenide (In_2Se_3) was selected due to its high resistivity ratio and lower programming current. Au/In_2Se_3-nanowire/Au phase change memory devices were fabricated and measured systematically in an *in situ* transmission electron microscope to perform a RESET/SET process under pulsed and dc voltage swept mode, respectively. During the switching, we observed the dynamic evolution of the phase transformation process. The switching behavior resulted from crystalline/amorphous change and revealed that a long pulse width would induce the amorphous or polycrystalline state by different pulse amplitudes, supporting the improvement of the writing speed, retention, and endurance of PCRAM.



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In the past decade, the dimensions of device structures have been miniaturized and followed Moore's law for better performance. One of the nonvolatile functionalities for the next generation was proposed to be phase change memory. With its simple structure, high density, fast speed, scaling limit, and low power consumption, phase change random access memory (PCRAM) is a potential candidate for replacing flash memory. The structure of PCRAM was composed of a phase change material, such as $Ge_2Sb_2Te_5$ (GST), AgInSbTe, or In_2Se_3, sandwiched between two electrodes. Among them, In_2Se_3 is of high resistivity ratio and lower programing current compared with GST.[1−6] It has two kinds of typical structures, vertical cell/thin film PRAM and horizontal cell/nanowire memory.[7] The former has a heater at the bottom, which is surrounded by dielectric materials and is easy to produce. The latter has high scalability, is self-assembled, and has reduced thermal budget and power consumption due to the smaller volume.[2,4,8−13] The heated area of the nanowire-based horizontal cell is confined to the phase change material, and the evolution of the phase change process could be observed and studied easily.[7]

Chalcogenide, the universal phase change material, has two polymorphic states, amorphous and crystalline. The amorphous state has a higher resistance for its short atomic range order, low free electron density, and high activation energy, while the crystalline state has lower resistance for its long-range atomic order, high free electron density, and low activation energy.[8] The switching of these two states is the important operation for the memory. In order to induce the phase transition, a high voltage and short pulse were applied to cause the crystalline state to switch to the amorphous state, while a low voltage and long pulse were applied to turn the amorphous state to a crystalline state.[6]

* Address correspondence to wwwu@mail.nctu.edu.tw.

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The basic mechanism has been studied to improve the characteristics of PCRAM.[14] However, the correlation between electrical behaviors and the evolution of the polymorphism is still unclear. In this work, we studied the real-time switching behavior of In_2Se_3 nanowire-based PCRAM in an *in situ* TEM. The evolution of the nanostructure within a nanowire was observed during the SET and RESET processes by pulsed and dc modes. This observation demonstrated that a long pulse width would induce the amorphous or polycrystalline state by different pulse amplitudes, providing the information to improve the writing speed, retention, and endurance of the PCRAM.

RESULTS AND DISCUSSION

The structure and chemical composition of In_2Se_3 nanowires were identified by transmission electron microscopy (TEM), energy-dispersive X-ray spectroscopy (EDS), and X-ray diffraction (XRD). The TEM image in Figure 1a shows that the diameter and the length of the In_2Se_3 nanowire were about 50 nm and several micrometers, respectively. The corresponding high-resolution TEM image and the fast Fourier transform (FFT) electron diffraction pattern of the marked area are highlighted in Figure 1b, indicating the [301] growth direction of the γ-phase single-crystal nanowire. Figure 1c is the EDS spectrum, and a table of indium/selenium ratio is in the inset, revealing that the ratio of indium and selenium was ~2:3. The XRD pattern also confirms that the as-grown In_2Se_3 nanowires were γ-phase, which is stable at room temperature and suitable for the phase change memory application as compared with β, δ, and κ, as shown in Supporting Information Figure S1. Figure 1d is the schematic crystal structure of the γ-phase In_2Se_3.

To understand the phase change switching behavior of In_2Se_3 nanowire memory devices, a series of electrical measurements were performed. Figure 2 shows the typical TEM image and electrical characteristics of several Au/In_2Se_3 nanowire/Au memory devices. The endurance of 800 cycles under a constant 0.1 V readout demonstrates that the resistance was 10^9 Ω at the high-resistance state, while the resistance was around 10^4 to 10^5 Ω at the low-resistance state. Although the low-resistance state fluctuates, the ratio of the amorphous and crystalline state still remains at 4 orders of magnitude among these devices. The corresponding RESET process is shown in Supporting Information Figure S2. To switch from the amorphous to single-crystalline state, the dc voltage sweep mode was applied (Figure 2c). The resistance changed from 1.95×10^7 to 4×10^4 Ω during a voltage sweep from 0 to 25 V. In this case, 5.6 μm electrode spacing would result in high-threshold SET voltage. The TEM images in the inset depict the structure evolution of the corresponding SET process. For the RESET process, a pulsed mode was applied to switch the device to induce a fast and sequence-like quench. If the crystal would have time to recrystallize, the amorphism process would fail.[7,15−20] The repeated switching of individual In_2Se_3 nanowire memory devices is shown in Figure 2d, while the R_{OFF}/R_{ON} ratio was stable for 10^5 orders under a constant 17 V readout. The evolution of atomic structure and SAED pattern varies in different devices,

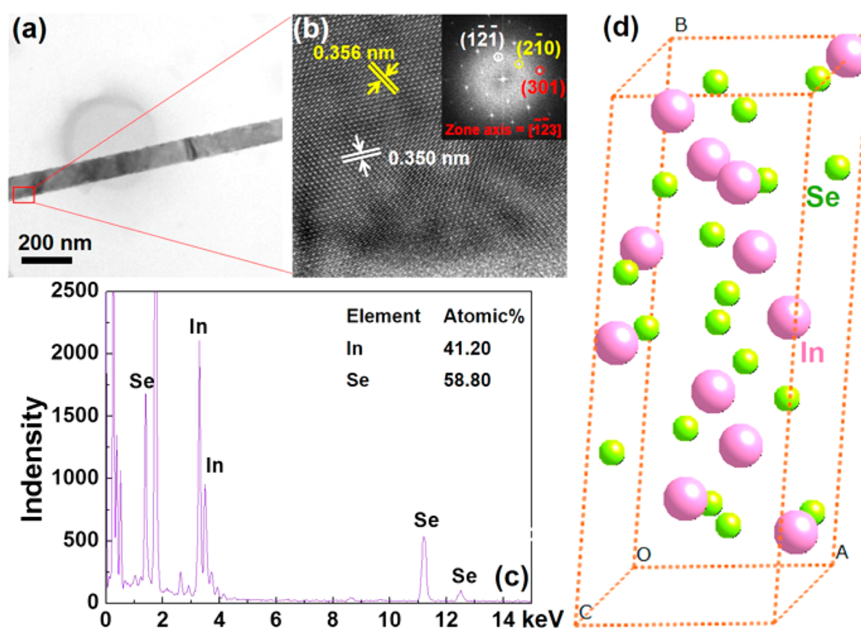

Figure 1. (a) TEM image of an In_2Se_3 nanowire of several micrometers in length and 50 nm in diameter. (b) High-resolution transmission electron microscope (HRTEM) image of the marked area in (a). The inset shows the corresponding FFT electron diffraction pattern with [−1−23] zone axis. (c) EDS spectrum with the corresponding atomic percentage of In and Se in the inset. (d) Schematic crystal structure of γ-phase In_2Se_3 nanowires.

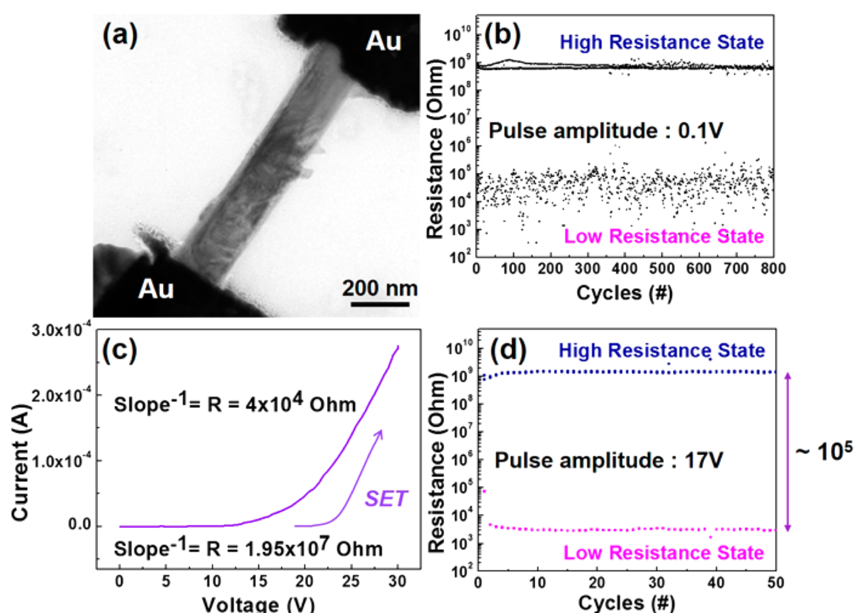

Figure 2. (a) TEM image of a Au/In_2Se_3 nanowire/Au memory device. (b) Endurance test under a constant 0.1 V readout. (c) Typical current−voltage measurement by voltage sweep to SET the In_2Se_3 nanowire memory. (d) In_2Se_3 nanowire memory device measured by pulsed mode to RESET under a constant 17 V readout with 10^5 R_{OFF}/R_{ON} ratio.

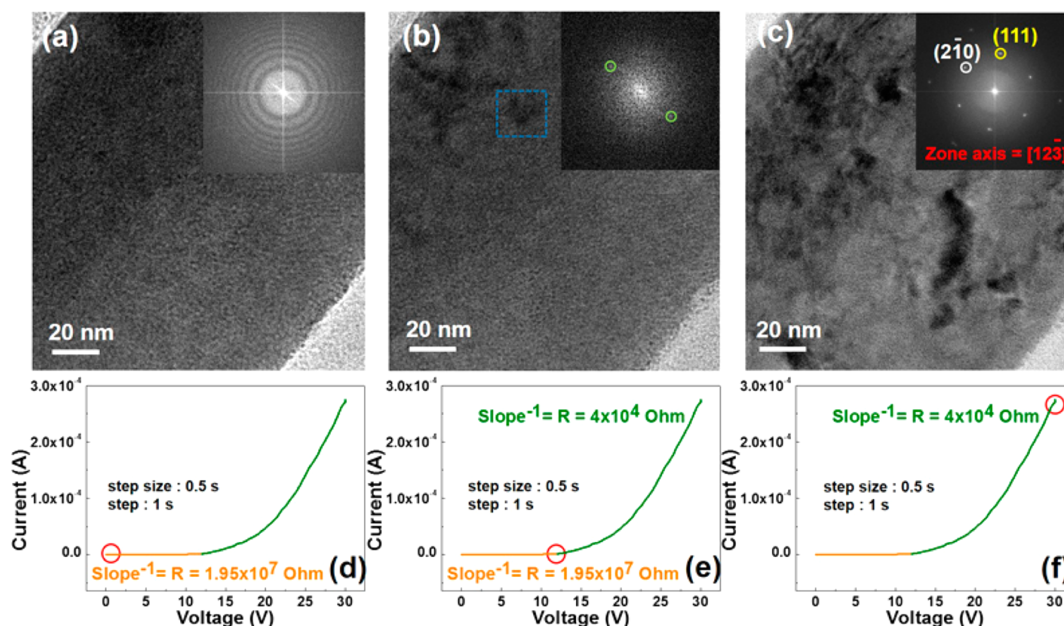

Figure 3. TEM images of the (a) original state, (b) crystalline state, and (c) single-crystalline state of the In_2Se_3 nanowire during phase transformation by dc voltage sweep mode to SET for a PCRAM device. (d−f) Corresponding current−voltage measurements.

depending on the pulse amplitude and width. The results of electrical measurements in Figure 2 show that the In_2Se_3 nanowire is a potential candidate for a phase change material.

Figure 3a−c present the structure evolution during a SET process, and the corresponding dc voltage sweep-mode behavior is highlighted with a red circle in Figure 3d−f.[6] During the process, which is shown in Supporting Information Video S1, the phase of the In_2Se_3 nanowire transformed from an amorphous state to a single-crystalline state, and the inset is the corresponding FFT electron diffraction pattern. Initially, the resistance of In_2Se_3 nanowire was 1.95×10^7 Ω. It was transformed by ion implantation; with the sub-electrodes fabricated by focus ion beam technology (FIB), the ion implantation (30 keV) at a higher dose may induce a phase transformation to an amorphous state.[21] After applying 12.5 V, the In_2Se_3 nanowire was partly crystallized. Finally, the In_2Se_3 nanowire transformed into single crystalline with a [12−3] zone axis

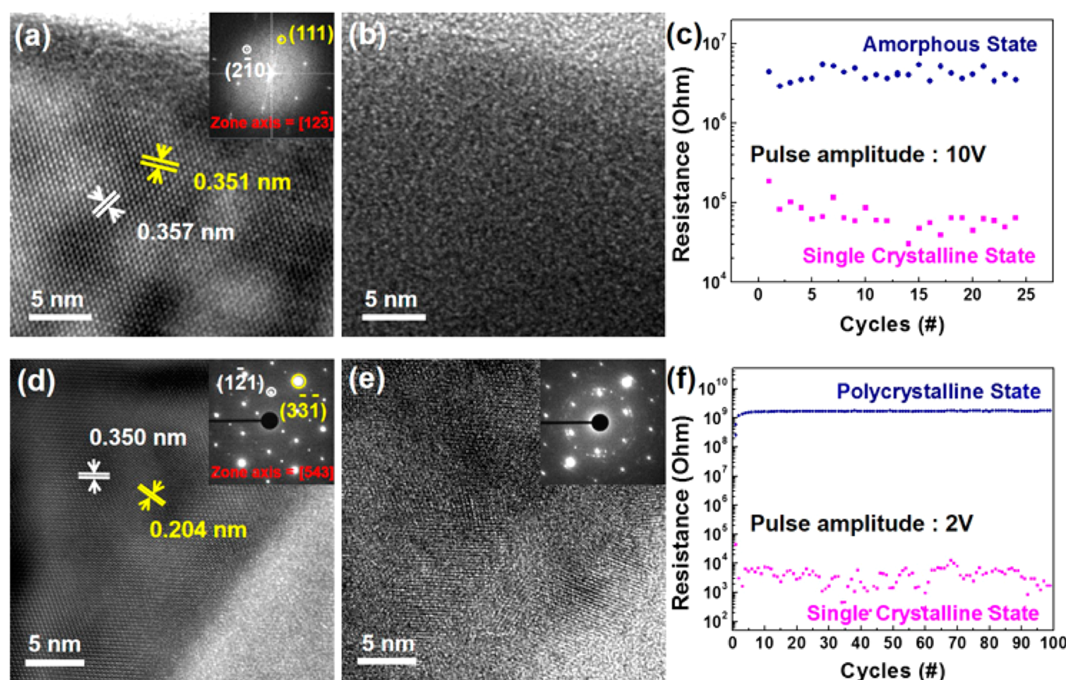

Figure 4. Phase transformation by pulsed mode switching to RESET the In_2Se_3 nanowire PCRAM. The In_2Se_3 nanowire changed from (a) single crystalline to (b) amorphous state. (d) Another example of the transformation from single crystalline state to (e) polycrystalline state after switching. (c and f) Corresponding electrical measurements, respectively.

after 25 V was applied. Meanwhile, its resistance was decreased to 4×10^4 Ω. This result demonstrated that the SET process was caused by the phase change from an amorphous state to a single-crystalline state.

For phase change memory materials, chalcogenide compounds have already exhibited quick switching ability.[1,6−8,22−26] In a SET transition, nucleation and growth processes are essential to the crystallization. When the voltage is applied, the duration time should be long enough to generate the heat for nucleation and growth. Then the material will transform and reach the low-resistance state. Thus, the temperature must be higher than its recrystallization temperature. Therefore, the dc voltage sweep mode was selected to apply in our experiments. From these images, it can be found that the nucleation and growth process occurred at low bias. The resistance decreased dramatically owing to full recrystallization and Joule heating. During the RESET−SET transition process, the temperature must be higher than the crystalline temperature and lower than the melting temperature; otherwise, the material cannot turn into the low-resistance state.[19,27,28] In our In_2Se_3 nanowire memory device, the distance between two electrodes was 5.6 μm, which is much longer than that of other reports, resulting in a larger threshold voltage of 25 V. This result also indicates that the magnitude of the electric field is another important factor for the phase change material to obtain the switching energy.

The pulsed mode was applied to RESET the In_2Se_3 nanowire memory in order to avoid recrystallization. During the process, the pulse width was set at 0.1 s in our study due to the instrumental limit. Figure 4a illustrates another example of single-crystalline In_2Se_3 nanowire with a [12−3] zone axis. After applying a pulse of 10 V for several cycles, the In_2Se_3 nanowire transformed into an amorphous state as shown in Figure 4b, and its resistance increased to 10^6 Ω. The corresponding electrical characteristic is shown in Figure 4c. We used a high, 200 keV electron dose. According to Figure S2, the phase transformed at many parts, but only the section pointed out by the red arrow was focused. The magnification was set at 600k. After the voltage was applied, the magnification was set at 25k to observe the evolution of the nanowires, showing that the phase change section appeared not only under the electron beam but also without it. Therefore, the electron beam has a negligible or no effect on the phase transition. Figure 4d illustrates another RESET example with a different zone axis, transforming into a polycrystalline state (Figure 4e and the corresponding video as shown in Supporting Information Videos S2) by a pulse of 2 V. The corresponding switching behavior and the endurance are shown in Figure 4f. The endurance was tested for 100 cycles with a stable R_{OFF}/R_{ON} ratio (10^6). Further investigations can be found in the Supporting Information (Figures S3 to S5 and Videos S2 to S4). From these results, a higher R_{OFF}/R_{ON} ratio from single-crystalline switching to polycrystalline was found. The higher resistance in the polycrystalline state compared with the amorphous state may result from the full transformation of the polycrystalline state rather than the partial transformation to the amorphous state in the nanowire. For a

longer pulse width, a much higher voltage should be applied to completely transform the nanowire into an amorphous state.[16] Grain boundary scattering may be another reason for the higher resistance of the polycrystalline state. While the grain size is smaller than or similar to the electron mean free path, the grain boundary will induce electron scattering, which will increase the resistivity of the polycrystalline nanowires.[29−31] Thus, the R_{OFF}/R_{ON} ratio from single-crystalline switching to the amorphous state in our study would be low.

In the SET−RESET transition, the amorphization was believed to be the melt−quench mechanism. The In_2Se_3 material should be heated quickly to high temperature and then rapidly cooled, so that the atoms can maintain disorder to reach an amorphous state with high resistance. Therefore, the pulsed mode with high amplitude and short pulse width was selected to RESET the In_2Se_3 phase change memory.[7,17,28,32,33] To reach a high temperature, a strong electric field would be necessary. This means that a stronger electric field can lead to a higher level of amorphization.[4] In Figure 4c and f, the pulse amplitudes were different. The higher pulse amplitude would cause the phase transition to be the amorphous state, while a lower one would induce the polycrystalline state. On comparison with the polycrystalline state and amorphous state for a RESET, the former was growth-dominated, while the latter was nucleation-dominated. Thus, a higher pulse voltage should be applied to the former to grow. Under the condition of long pulse width and small pulse amplitude, the temperature was not high enough to reach a crystalline state immediately, and the low-resistance state would be less stable[15,34] (more details in Supporting Information Figures S3 to S5). In previous studies, a RESET to polycrystalline state has never been found, which may be caused by the longer pulse width. Under this condition, the temperature was high enough to melt the phase change material without a large pulse amplitude. Meanwhile, the longer pulse width would result in the annealing process instead of a quench process and arrange the atoms. As the In_2Se_3 nanowire was partly transformed from single crystalline to polycrystalline, the larger pulse amplitude made the large area transform to polycrystalline. Furthermore, due to the induction of higher temperature, the grain size was larger while the larger pulse amplitude was applied (more details in Supporting Information Figure S6). Our observation provides the evidence for the correlation between electric behaviors of SET/RESET processes and the evolution of nanostructures. Apparently, the pulse width and amplitude, which induce different magnitudes of electric fields, will affect the transformation from single crystalline to different phases.

CONCLUSIONS

In conclusion, we have fabricated In_2Se_3 nanowire-based phase change memory devices of high resistivity ratio and lower programming current. The devices were switched by dc voltage sweep mode and pulsed mode. We observed the structural evolution of the In_2Se_3 nanowire by *in situ* TEM and found that different pulse amplitudes and widths would result in phase transformation to polycrystalline or amorphous states. This study is expected to enhance the writing speed, retention, and endurance of PCRAM for future applications.

METHODS

In_2Se_3 nanowires were synthesized in a vacuum furnace by the vapor−liquid−solid mechanism. A 0.82 g amount of selenium powder was placed upstream, while 1.2 g of indium shot was placed downstream with a 2 nm Au coated silicon substrate placed nearby. The temperature was kept for 2 h at 240 and 600 °C, respectively. The vacuum of the system was kept at 1 Torr with 200 sccm argon flow. After the growth processes, In_2Se_3 nanowires were grown on the substrates.

A 30 nm SiO_2 and a 60 nm Si_3N_4 layer were deposited on the Si substrate by a low-pressure chemical vapor deposition system. The region at the bottom window and the main electrode at the top were defined by photolithography. Then the bottom region was etched with KOH solution, leaving a Si_3N_4 window for TEM inspection. A 20 nm Ti and a 40 nm Au layer were deposited by an electron gun evaporation system (E-gun) as the main electrode. A 30 nm Ti and 120 nm Au subelectrode were fabricated by the electron-beam lithography process and E-gun to form the In_2Se_3-PCRAM. The sample fabrication process and the corresponding SEM image of the device are shown in Supporting Information Figure S7. Subelectrodes were also fabricated by FIB, and a 100 nm Pt layer was deposited. The subelectrodes of different metals, Au and Pt, did not influence the electrical behavior due to the following two points. The first one is that Au and Pt are inert metals that will not react with In_2Se_3 nanowires. The other one is that the resistance of In_2Se_3 nanowires was about 10^4 ohm for all the electrodes. According to our previous experiments on nanowire electrical measurements, the order of resistance was the same with Au and Pt as subelectrodes. *In situ* TEM observation was carried out in a JEOL ARM-200FTH TEM, which was equipped with a video recorder with a 1/30 s time resolution and EDS. The *IV* switching behavior was operated by Protochips Aduro 300.[35−37]

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Identification of In_2Se_3 nanowires, *in situ* TEM images, and electrical measurements as supplementary online materials present the observation of the In_2Se_3-PCRAM during the RESET process. *In situ* TEM videos provide direct evidence of the In_2Se_3 nanowire phase transformation processes. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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